Xing-ru Peng, Wei Zhang, Yan-yan Liu, 2016. A pipelined Reed-Solomon decoder based on a modified step-by-step algorithm. *Frontiers of Information Technology & Electronic Engineering*, **17**(9):954-961.
http://dx.doi.org/10.1631/FITEE.1500303

A pipelined Reed-Solomon decoder based on a modified step-by-step algorithm

Key words: Reed-Solomon codes, Step-by-step algorithm, Ultra-wideband, Pipelined structure

Corresponding author: Yan-yan Liu
E-mail: lyytianjin@nankai.edu.cn
ORCID: http://orcid.org/0000-0001-8488-5480

Motivation

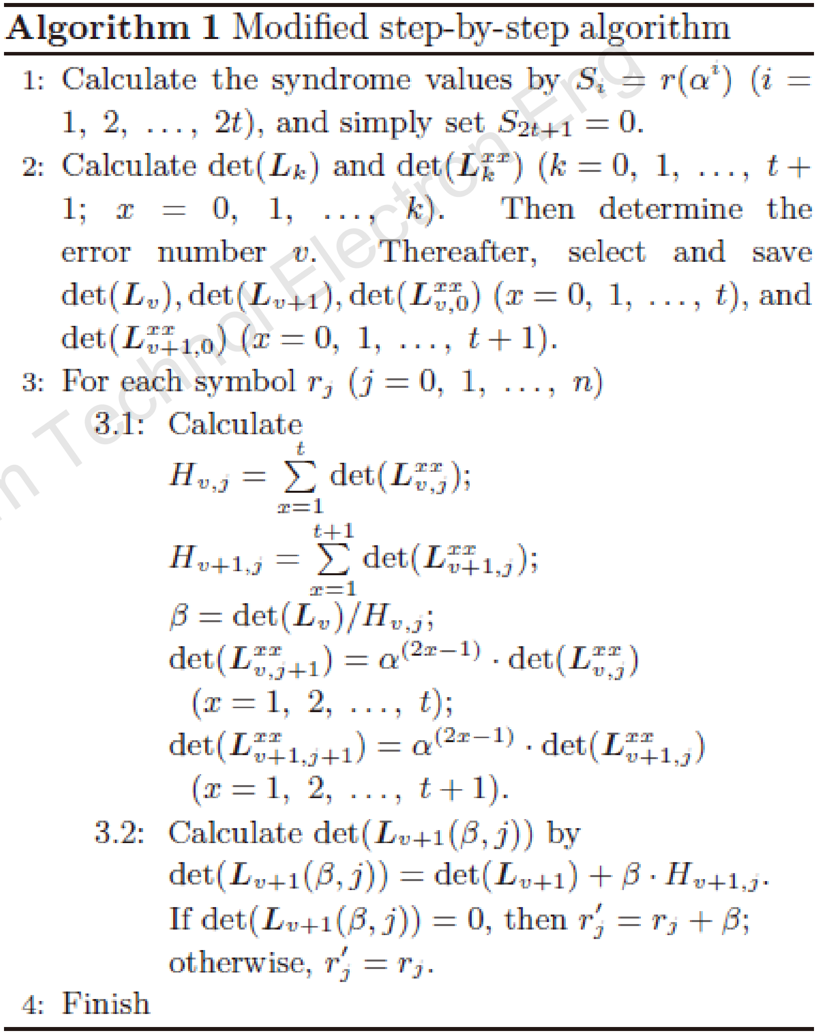
- The most well-known decoding methods for RS codes share three main steps: syndrome calculator (SC), key equation solver (KES), and Chien search and error evaluator (CSEE).
- Massey (1965) presented a totally different decoding algorithm, can directly determine whether the received symbol is erroneous or not and immediately find the corresponding error value without solving the key equations.
- However, Chen *et al*. (2000) and Liu *et al*. (2007) took two different ways to decode when the error number is equal to t or not, which involve a lot of redundant operations.

Main idea

- A modified step-by-step algorithm is proposed, which merges the two cases and hence reduces the complexity significantly.
- Since the SC block takes a long time, rather than reducing the latency efficiently, the parallel algorithm (Liu *et al*., 2007) increases the hardware requirements. In this paper, a pipelined architecture is proposed. This architecture does not introduce extra latency while reducing hardware complexity, which increases the hardware utilization efficiency significantly.

Method

- A modified step-by-step algorithm is proposed.



Algorithm 1 Modified step-by-step algorithm

```
1: Calculate the syndrome values by $S_i = r(\alpha^i)$ $(i = 1, 2, \ldots, 2t)$, and simply set $S_{2t+1} = 0$.
2: Calculate $\det(L_k)$ and $\det(L_k^{xx})$ $(k = 0, 1, \ldots, t+1;\ x = 0, 1, \ldots, k)$. Then determine the error number $v$. Thereafter, select and save $\det(L_v), \det(L_{v+1}), \det(L_{v,0}^{xx})$ $(x = 0, 1, \ldots, t)$, and $\det(L_{v+1,0}^{xx})$ $(x = 0, 1, \ldots, t+1)$.
3: For each symbol $r_j$ $(j = 0, 1, \ldots, n)$
    3.1: Calculate
         $H_{v,j} = \sum_{x=1}^{t} \det(L_{v,j}^{xx})$;
         $H_{v+1,j} = \sum_{x=1}^{t+1} \det(L_{v+1,j}^{xx})$;
         $\beta = \det(L_v)/H_{v,j}$;
         $\det(L_{v,j+1}^{xx}) = \alpha^{(2x-1)} \cdot \det(L_{v,j}^{xx})$
           $(x = 1, 2, \ldots, t)$;
         $\det(L_{v+1,j+1}^{xx}) = \alpha^{(2x-1)} \cdot \det(L_{v+1,j}^{xx})$
           $(x = 1, 2, \ldots, t+1)$.
    3.2: Calculate $\det(L_{v+1}(\beta, j))$ by
         $\det(L_{v+1}(\beta, j)) = \det(L_{v+1}) + \beta \cdot H_{v+1,j}$.
         If $\det(L_{v+1}(\beta, j)) = 0$, then $r_j' = r_j + \beta$;
         otherwise, $r_j' = r_j$.
4: Finish
```

Method

- 2. According to the modified step-by-step algorithm, a pipelined step-by-step decoder is proposed.

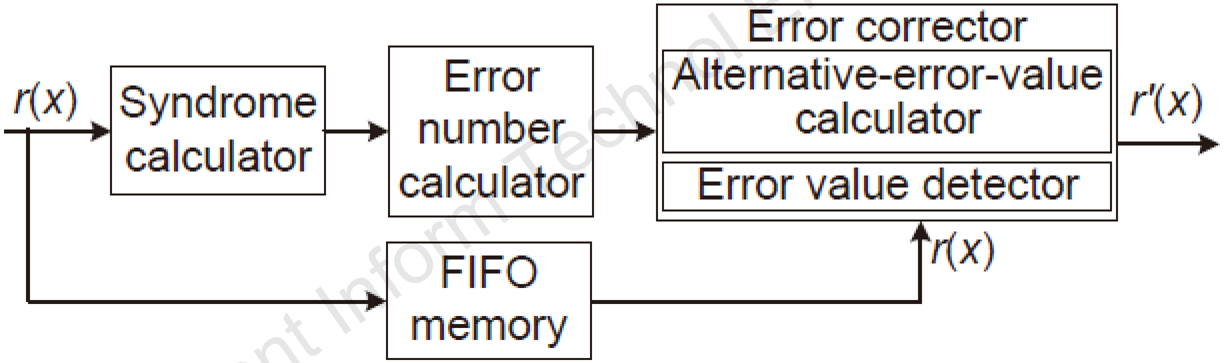


Fig. 3 Block diagram of the pipelined step-by-step decoder

Major results

- For RS(23,17) codes, the hardware requirement of the proposed architecture is 42.5%, 24.4%, and 11.3% less than that of ME, pDCME, and the previous SBS architecture, respectively.

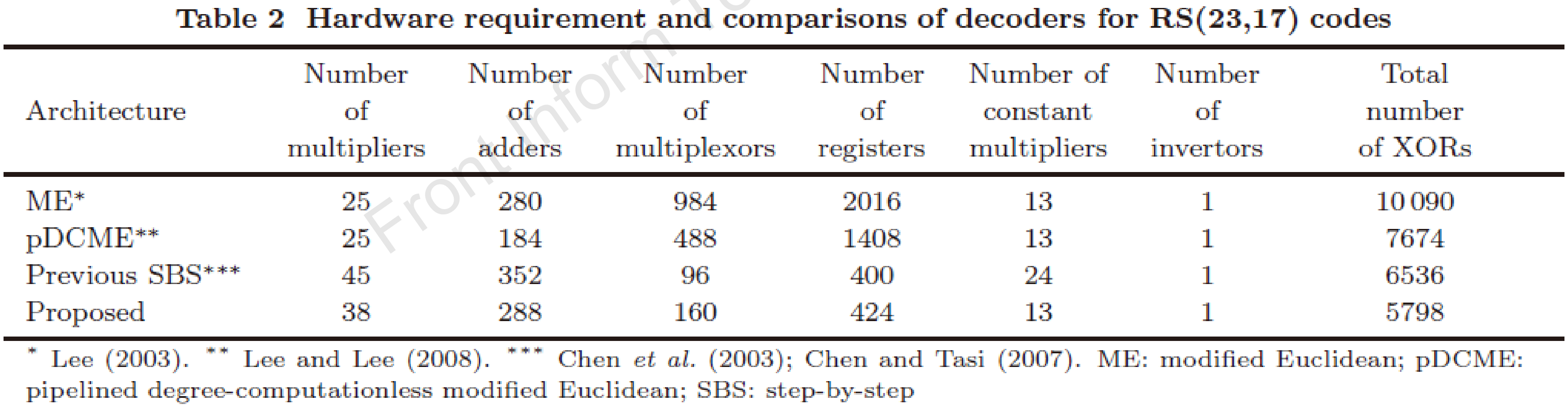


Table 2 Hardware requirement and comparisons of decoders for RS(23,17) codes

Architecture	Number of multipliers	Number of adders	Number of multiplexors	Number of registers	Number of constant multipliers	Number of invertors	Total number of XORs
ME*	25	280	984	2016	13	1	10 090
pDCME**	25	184	488	1408	13	1	7674
Previous SBS***	45	352	96	400	24	1	6536
Proposed	38	288	160	424	13	1	5798

* Lee (2003). ** Lee and Lee (2008). *** Chen *et al.* (2003); Chen and Tasi (2007). ME: modified Euclidean; pDCME: pipelined degree-computationless modified Euclidean; SBS: step-by-step

Major results

- The modified SBS algorithm can always achieve the same performance as the ME and SBS algorithms. That is to say, the modified SBS algorithm can significantly improve the hardware utilization without performance degradation.

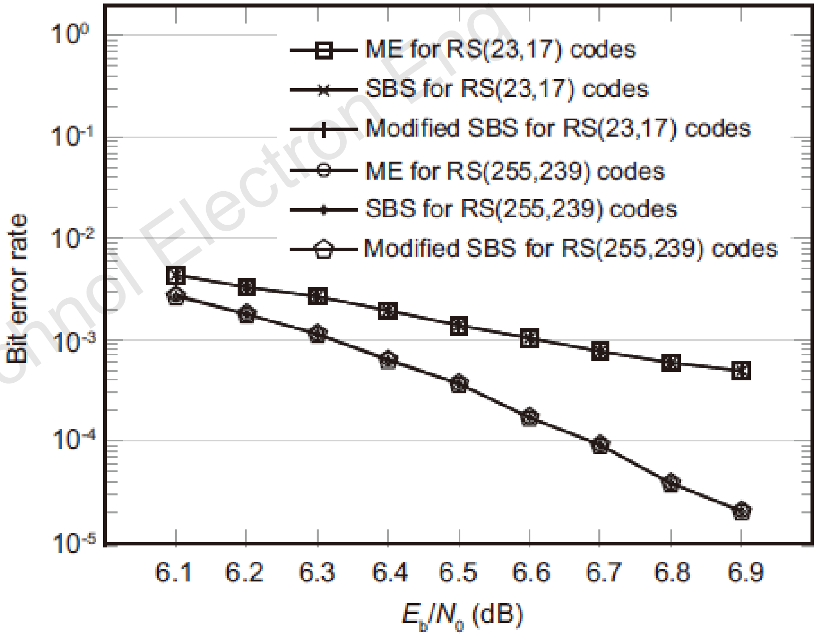


Fig. 10 Simulation results for RS codes decoding schemes

Conclusions

- A modified step-by-step algorithm and a novel pipelined decoder for RS(23,17) codes are proposed in this paper. With modification, the computational complexity is significantly reduced.
- In addition, much less area is needed for this decoder compared with the ME architecture and the pDCME architecture. As a result, the low computational and hardware complexities make the proposed decoder suitable for the UWB system.